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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,141	01/11/2002	Jong Sik Paek	AMKOR-018A	1112
7663	7590	05/07/2004	EXAMINER	
STETINA BRUNDA GARRED & BRUCKER			CHU, CHRIS C	
75 ENTERPRISE, SUITE 250			ART UNIT	
ALISO VIEJO, CA 92656			PAPER NUMBER	

2815

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/044,141	Applicant(s) PAEK, JONG SIK AK	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 January 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 21 and 27 - 31 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 21 and 27 - 31 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on January 26, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 102

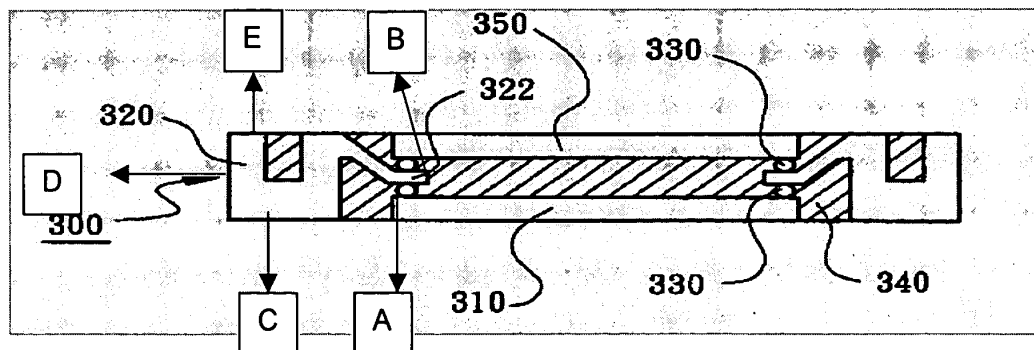
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 ~ 6 and 11 ~ 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Chun-Jen et al. '510.

Regarding claim 1, Chun-Jen et al. discloses in e.g., Fig. 5 a semiconductor package comprising:



- a plurality of leads (320), each of the leads defining:

- a generally planar first surface (A; the generally planar surface area where the solder ball 330 is not attached);
 - a generally planar second surface (B; the generally planar surface area where the solder ball 330 is not attached) disposed in opposed relation to the first surface; and
 - a generally planar third surface (C) disposed in opposed, substantially parallel relation to the second surface and laterally offset outwardly relative to the first surfaces;
- a first semiconductor die (310) defining opposed top and bottom surface;
 - a second semiconductor die (350) defining opposed top and bottom surfaces;
 - a plurality of conductive connectors (330) electrically and mechanically connecting the first semiconductor die to the first surfaces of the leads and the second semiconductor die to the second surfaces of the leads; and
 - an encapsulating portion (340) applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors such that at least the first and second surfaces of each of the leads are covered by the encapsulating portion.

Regarding claim 2, Chun-Jen et al. discloses in Fig. 5 and column 3, line 62 the conductive connectors each comprising a conductive bump (330).

Regarding claim 3, Chun-Jen et al. discloses in Fig. 5 and column 2, line 38 the conductive bump being fabricated from material selected from solder.

Regarding claim 4, Chun-Jen et al. discloses in Fig. 5

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- the first semiconductor die (310) includes a plurality of bond pads (an area directly under the solder ball 330, at the top) disposed on the top surface thereof;
- the second semiconductor die (350) includes a plurality of bond pads (an area directly under the solder ball 330, at the bottom) disposed on the bottom surface thereof; and
- the conductive connectors (330) are used to electrically and mechanically connect the bond pads of the first semiconductor die to respective ones of the first surfaces of the leads and the bond pads of the second semiconductor die to respective ones of the second surfaces of the leads.

Regarding claim 5, Chun-Jen et al. discloses in Fig. 5 the conductive connectors each comprising a conductive bump.

Regarding claim 6, Chun-Jen et al. discloses in Fig. 5

- each of the leads (320) includes a first bump land formed at a prescribed region of the first surface thereof and a second bump land formed at a prescribed region of the second surface thereof;
- the conductive connectors (330) each comprise a conductive bump; and
- the conductive bumps are fused to respective ones of the first and second bump lands of each of the leads.

Regarding claim 11, Chun-Jen et al. discloses in Fig. 5 the first and second semiconductor dies being identically sized.

Regarding claim 12, Chun-Jen et al. discloses in Fig. 5 the encapsulating portion being applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion.

Regarding claim 13, Chun-Jen et al. discloses in Fig. 5 the encapsulating portion (340) being applied to the first and second semiconductor dies such that the bottom surface of the first semiconductor die and the top surface of the second semiconductor die are each exposed within the encapsulating portion.

Regarding claim 14, Chun-Jen et al. discloses in Fig. 5 the leads and the first semiconductor die being oriented relative to each other such that the bottom surface of the first semiconductor die is substantially flush with the third surface of each of the leads.

Regarding claim 15, Chun-Jen et al. discloses in Fig. 5

- each of the leads (320) further defines an outer end (D) which extends between the second and third surfaces thereof; and
- the encapsulating portion is applied to the leads such that the outer end of each of the leads is exposed within the encapsulating portion.

Regarding claim 16, Chun-Jen et al. discloses in Fig. 5 each of the leads (320) further defines a fourth surface (E) disposed in opposed relation to the third surface and laterally offset outwardly relative to the second surface.

Regarding claim 17, Chun-Jen et al. discloses in Fig. 5 the encapsulating portion being applied to the leads such that the third and fourth surfaces of each of the leads are exposed within the encapsulating portion.

Regarding claim 18, Chun-Jen et al. discloses in Fig. 5 the encapsulating portion being applied to the first and second semiconductor dies such that the bottom surface of the first semiconductor die and the top surface of the second semiconductor die are each exposed within the encapsulating portion.

Regarding claim 19, Chun-Jen et al. discloses in Fig. 5 the second semiconductor die and the leads being oriented relative to each other such that the top surface of the second semiconductor die is substantially flush with the fourth surface of each of the leads.

Regarding claim 20, Chun-Jen et al. discloses in Fig. 5 the first semiconductor die and the leads being oriented relative to each other such that the bottom surface of the first semiconductor die is substantially flush with the third surface of each of the leads.

Regarding claim 21, Chun-Jen et al. discloses in Fig. 3, Fig. 5 and column 3, line 56 ~ column 4, line 2 further in combination with a second semiconductor package identically configured to the semiconductor package, the third surfaces of the leads of the second semiconductor package being electrically connected to respective ones of the fourth surfaces of the leads of the semiconductor package.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun-Jen et al. in view of Takahashi (JP-05206219).

Regarding claims 7 and 9, Chun-Jen et al. discloses the claimed invention except for each of the leads including first and second protective layers on the bump land. However, Takahashi

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teaches in e.g., Fig. 1, Fig. 3 and abstract, lines 1 - 28 each of the leads (10) including a first protective layer (13, at the left) coated on the first surface thereof about a respective one of conductive connectors (17); and a second protective layer (13, at the right) coated on the second surface thereof about a respective one of conductive connectors (17). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Chun-Jen et al. by using first and second protective layers as taught by Takahashi. The one of ordinary skill in the art would have been motivated to modify Chun-Jen et al. in the manner described above for at least the purpose of preventing short-circuit (abstract, lines 26 ~ 28).

6. Claims 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun-Jen et al. and Takahashi as applied to claims 7 and 9 above, and further in view of Lee '074.

Regarding claims 8 and 10, while Takahashi teaches the use of the lead finger protective layers, Takahashi does not appear to provide any example of the protective layer's specific composition. Lee teaches in e.g., Fig. 12 and column 7, lines 58 – 60 the protective layers (11) may be composed of a polyimide. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the polyimide as the specific material to form the protective layers on the lead fingers of Chun-Jen et al. and Takahashi as taught by Lee to prevent electrical coupling between the chip and the lead fingers (column 8, lines 37 – 40).

7. Claims 27 – 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chun-Jen et al. in view of Takahashi (JP-05206219).

Regarding claim 27, Chun-Jen et al. discloses in e.g., Fig. 5 a semiconductor package comprising:

- a plurality of leads (320);
- a portion of the leads define a land (an area directly under the solder ball 330);
- first (310) and second (350) semiconductor dies electrically and mechanically connected to the leads in opposed relation to each other through the use of a plurality of conductive connectors (330) which abut respective ones of the lands; and
- an encapsulating portion (340) applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors such that portions of the leads are exposed in a common exterior surface of the encapsulating portion.

Chun-Jen et al. discloses the claimed invention except for a plurality of protective layers. However, Takahashi teaches in e.g., Fig. 1, Fig. 3 and abstract, lines 1 - 28 a plurality of protective layers (13, at the left and right sides) disposed on respective ones of the leads (10), each of the protective layers being configured such that a portion (at the place of the element 17) of a corresponding one of the leads is exposed therein so as to define a land. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Chun-Jen et al. by using the plurality of protective layers on the leads as taught by Takahashi. The one of ordinary skill in the art would have been motivated to modify Chun-Jen et al. in the manner described above for at least the purpose of preventing short-circuit (abstract, lines 26 ~ 28).

Regarding claim 28, Chun-Jen et al. discloses in Fig. 5 a portion of one of the first and second semiconductor dies being exposed in the exterior surface of the encapsulating portion.

Regarding claim 29, Chun-Jen et al. discloses in Fig. 5 the encapsulating portion defining an opposed pair of exterior surfaces, and portions of the first and second semiconductor dies being exposed in respective ones of the exterior surfaces.

Regarding claim 30, Chun-Jen et al. discloses in Fig. 5 a semiconductor package comprising:

- a plurality of leads (320);
- a portion of the leads define a land (an area directly under the solder ball 330);
- first (310) and second (350) semiconductor dies electrically and mechanically connected to the leads in opposed relation to each other through the use of a plurality of conductive connectors (330) which abut respective ones of the lands; and
- an encapsulating portion (340) applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors such that portions of each of the leads are exposed in respective ones of an opposed pair of exterior surfaces of the encapsulating portion.

Chun-Jen et al. discloses the claimed invention except for a plurality of protective layers. However, Takahashi teaches in e.g., Fig. 1, Fig. 3 and abstract, lines 1 - 28 a plurality of protective layers (13, at the left and right sides) disposed on respective ones of the leads (10), each of the protective layers being configured such that a portion (at the place of the element 17) of a corresponding one of the leads is exposed therein so as to define a land. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to

modify Chun-Jen et al. by using the plurality of protective layers on the leads as taught by Takahashi. The one of ordinary skill in the art would have been motivated to modify Chun-Jen et al. in the manner described above for at least the purpose of preventing short-circuit (abstract, lines 26 ~ 28).

Regarding claim 31, Chun-Jen et al. discloses in Fig. 3, Fig. 5 and column 3, line 56 ~ column 4, line 2 further in combination with a second semiconductor package identically configured to the semiconductor package, at least some of the leads of the second semiconductor package being electrically connected to at least some of the leads of the semiconductor package.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 27 and 30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
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BRADLEY BAUMEISTER
PRIMARY EXAMINER